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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,047	01/31/2002	Steven Teig	SPLX.P0101	1989

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EXAMINER

TAT, BINH C

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/062,047

Applicant(s)

TEIG ET AL.

Examiner

Binh C. Tat

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05/22/2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

1. This office action is in response to application 10/062047 filed on 05/22/02.

Claims 1-14 remain pending in the application.

***Claim Objections***

2. Claim 1 line 8 should change “.” To “;”.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Pederson et al. (U.S. 6490717).

5. As to claim 1 Pederson et al. teach a method for performing technology mapping, the method comprising: a) receiving a design that is not bounded to a particular technology (see col 8 lines 16-30); b) repeatedly: selecting from the design a candidate sub-network, identifying at least one replacement sub-network from a storage structure that stores replacement sub-networks (see fig 3a and 3b col 9 lines 51-67 and col 10, 11);

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replacing the selected candidate sub-network in the design with the replacement sub-network (see fig 3a and 3b col 9 lines 51-67 and col 10, 11 and summary); c) wherein at least each of a first set of replacement sub-networks have multiple circuit elements, wherein each of the multiple circuit elements of a first-set replacement subnetwork is independently selectable by the method (see fig 3a, 3b, 7a-d col 9 lines 51-67 and col 10, 11, 14).

6. As to claims 2-5 Pederson et al. teach wherein identifying the replacement sub-network comprises: generating a parameter based on a set of output functions performed by the selected candidate sub-network, wherein the parameter identifies the replacement sub-network (see fig 3a and 3b col 9 lines 51-67 and col 10, 11).

7. As to claims 6-7 Pederson et al. teach terminating the repetitions once a stopping criteria is reached (see fig 3a and 3b col 9 lines 51-67 and col 10, 11); and wherein the design includes a plurality of circuit elements and the sub-networks are formed by circuit elements, the method further comprising: after terminating the repetitions, traversing the design to identify circuit elements that are not bound to the technology library (see fig 3a and 3b col 9 lines 51-67 and col 10, 11); for each identified circuit element, attempting to identify a replacement sub-network that is stored in the storage structure (see fig 3a and 3b col 9 lines 51-67 and col 10, 11); if at least one replacement sub-network for an identified circuit element is identified, replacing the circuit element in the design with the identified replacement sub-network (see fig 3a and 3b col 9 lines 51-67 and col 10, 11).

8. As to claims 8-9 Pederson et al. teach wherein if more than one replacement sub-networks are identified for a circuit element, selecting one of the replacement sub-networks and replacing the circuit element with the selected replacement

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sub-network (see fig 3a and 3b col 9 lines 51-67 and col 10, 11).

9. As to claim 10 Pederson et al. teach wherein each circuit element performs a function, wherein if no replacement sub-network is identified for an identified circuit element, decomposing the function of the circuit element into a set of functions, and then attempting to identify a set of replacement sub-networks in the storage structure that perform the set of functions (see fig 3a and 3b col 9 lines 51-67 and col 10, 11).

10. As to claims 11-12 Pederson et al. teach wherein traversing the design to identify circuit elements comprises identifying circuit elements that existed in the design when the design was received; after traversing the design, repeatedly: selecting from the design a candidate sub-network, identifying at least one replacement sub-network from a storage structure that stores replacement sub-networks, replacing the selected candidate sub-network in the design with the replacement sub-network (see fig 3a and 3b col 9 lines 51-67 and col 10, 11).

11. As to claims 13-14 Pederson et al. teach before replacing the candidate sub-networks with the replacement sub-networks, evaluating whether to replace the selected candidate sub-network with the replacement sub network, wherein certain candidate sub-networks are replaced by replacement sub-networks based on the evaluation, wherein certain candidate sub-networks are not replaced based on the evaluations (see fig 3a and 3b col 9 lines 51-67 and col 10, 11).

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***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat  
Art Unit 2825  
June 13, 2003

  
VUTHE SIEK  
PRIMARY EXAMINER